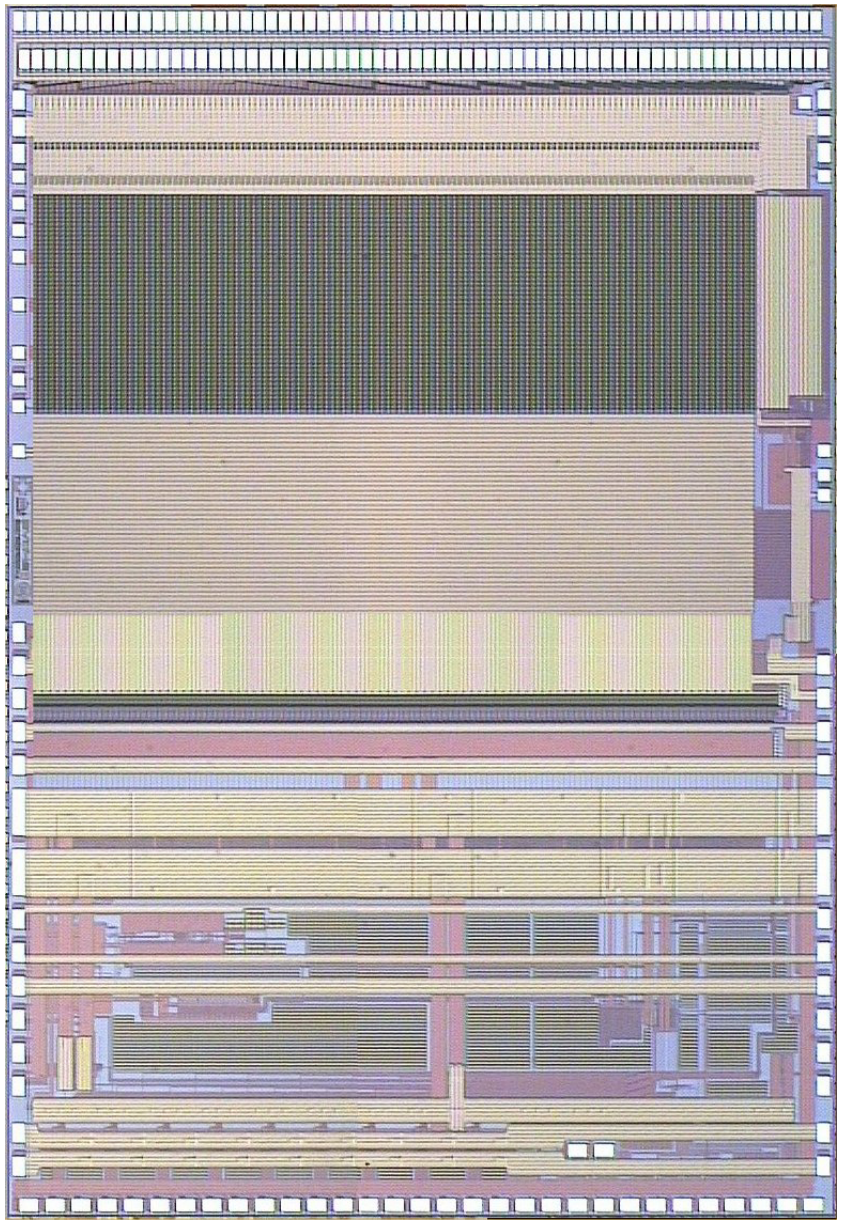
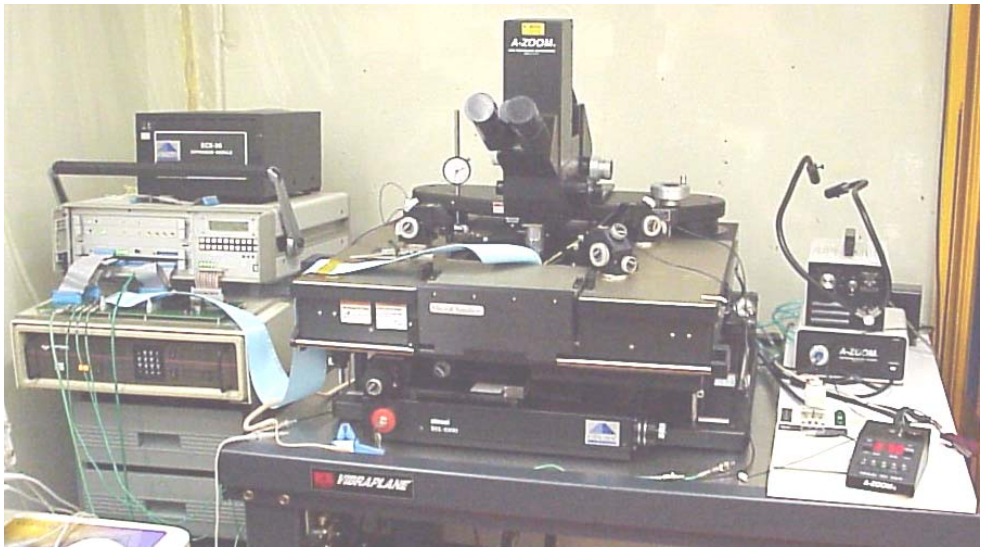


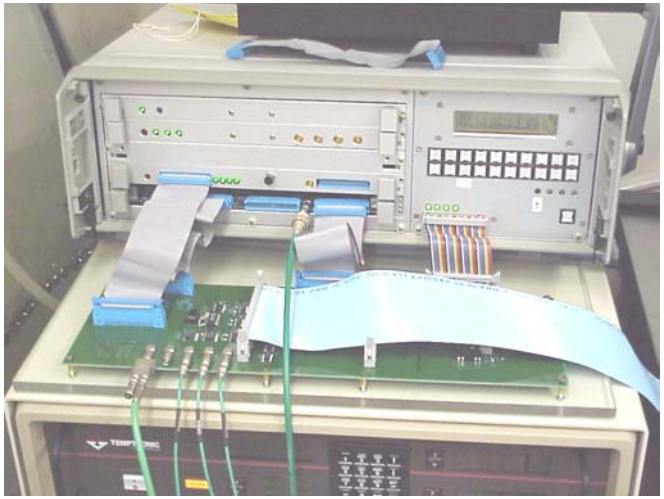
Wafer scale testing of SVX4

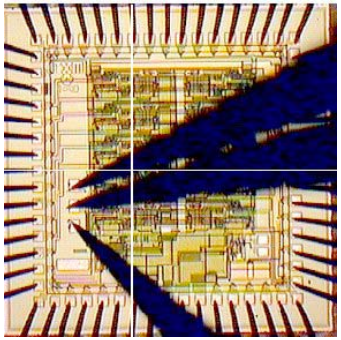
W. Wester
FNAL

I. ASIC Testing Lab
II. SVX4 History
III. V1 / V2 results
IV. 2a / 2b checks
V. 2a /2b probing
VI. Status and plans



Probe station under Windows software control (step from die-to-die). Serial connection with tester box that uses an interface PCB to supply AVDD and DVDD, measure currents and voltages. Actual DAQ is handled by a Linux based system developed at LBNL that uses PCI and ISA cards and PATT FIFO board.





The SVX4 chip for CDF/D0 in Run IIb

History:

2000: Only 0.25 μm makes sense
LBNL starts some design

2001: Official FNAL/LBNL project

2001: SVX4FE – FNAL front-end test chip works!

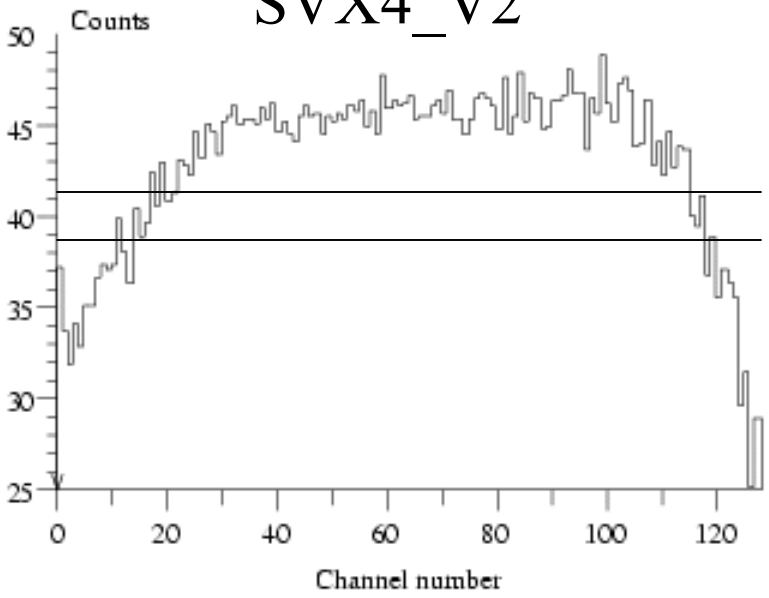
5/2002: SVX4_V1 and SVX4_V2 full-size prototypes work well. 97% of the parts are functional. 91% appear perfect (very high yield). Parts used for hybrid and stave prototypes.

5/2003: SVX4_V2a (back-up), SVX4_V2b (pre-production, but it's likely the production chip). Initial tests show high yields.

SVX4_V1 and V2 wafer probing

- 12 wafers total, 9 with probing results
  - (2 diced before tests, 1 with some suspect results)
- 9 wafers probed for current measurements
  - 18/936 chips fail with bad current draw on either AVDD or DVDD (i.e. shorts) (1.9%)
- ~7 wafers probed for basic functionality
  - 37/762 chips have a small problem (bad channel(s), fail sparsification, etc.) (4.3%)
- 3 V2 wafers tested fully (all pipeline cells etc.)
  - 4/156 chips have a very small problem (more than one bad pipeline cell, noisy, etc.) (2.6%)
- Overall yield: 91.2% perfect, 97% functional !

SVX4_V2



Extreme settings to highlight the bow:

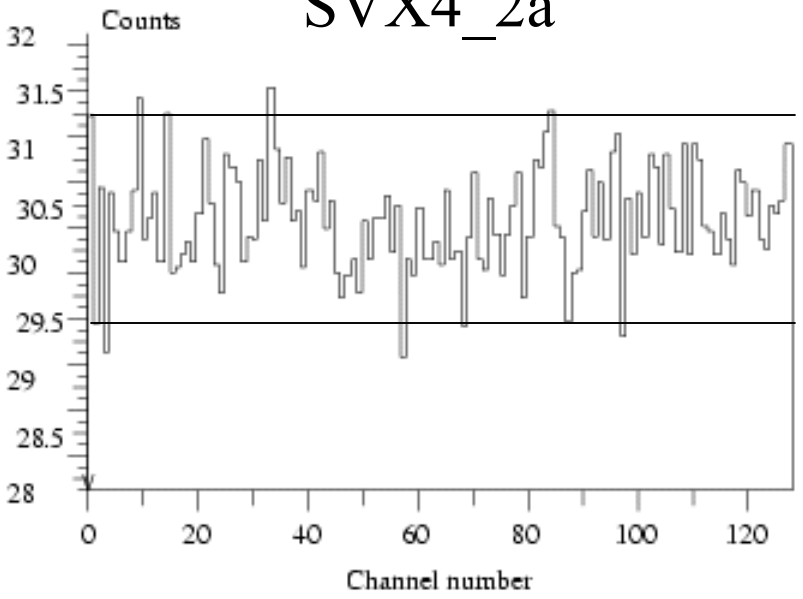
Minimize time between Comp and ramp resets

Ramp Ped set to max (lowest pedestal) or 9 for _V2 and 10 for _2x

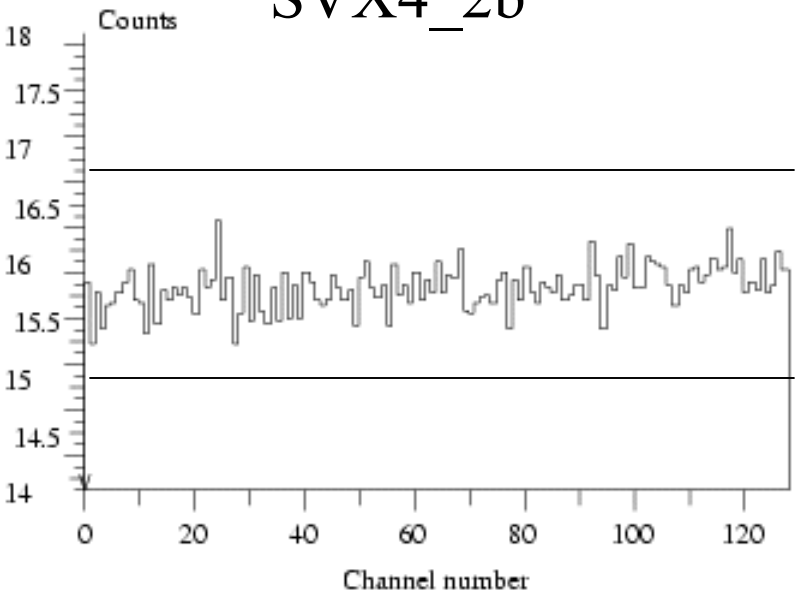
DVDD = 2.75 V (AVDD = 2.5 V)

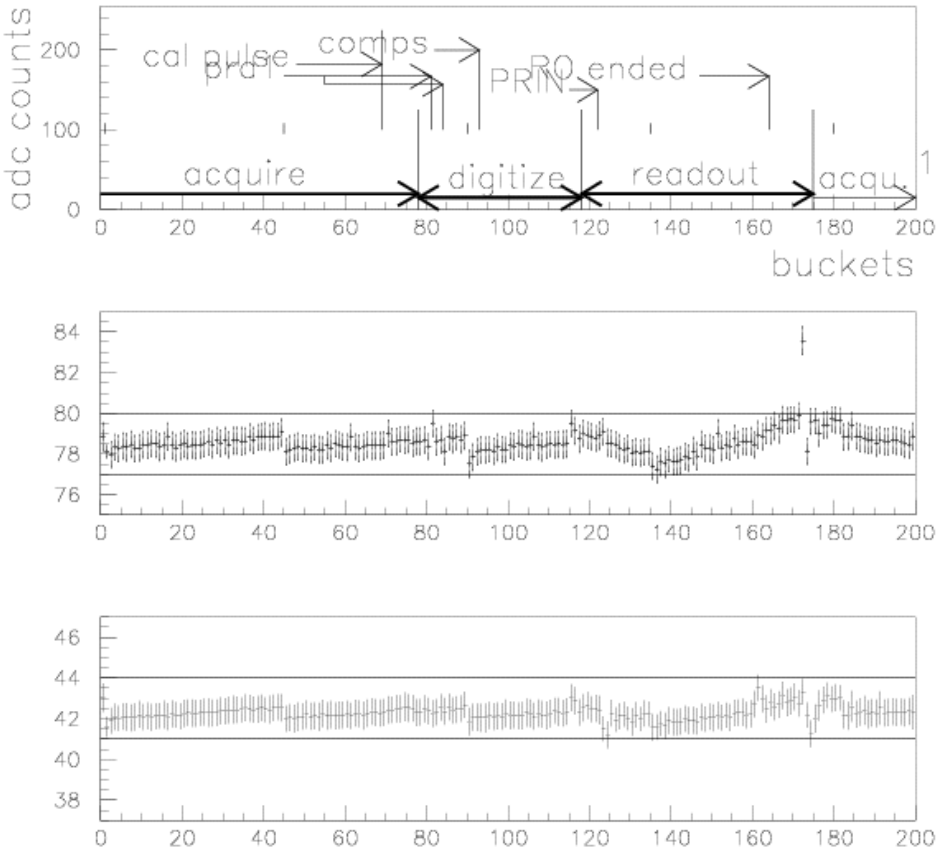
Offset of 15 cnts between _2a and_2b exists for other ramp ped settings.

SVX4_2a



SVX4_2b



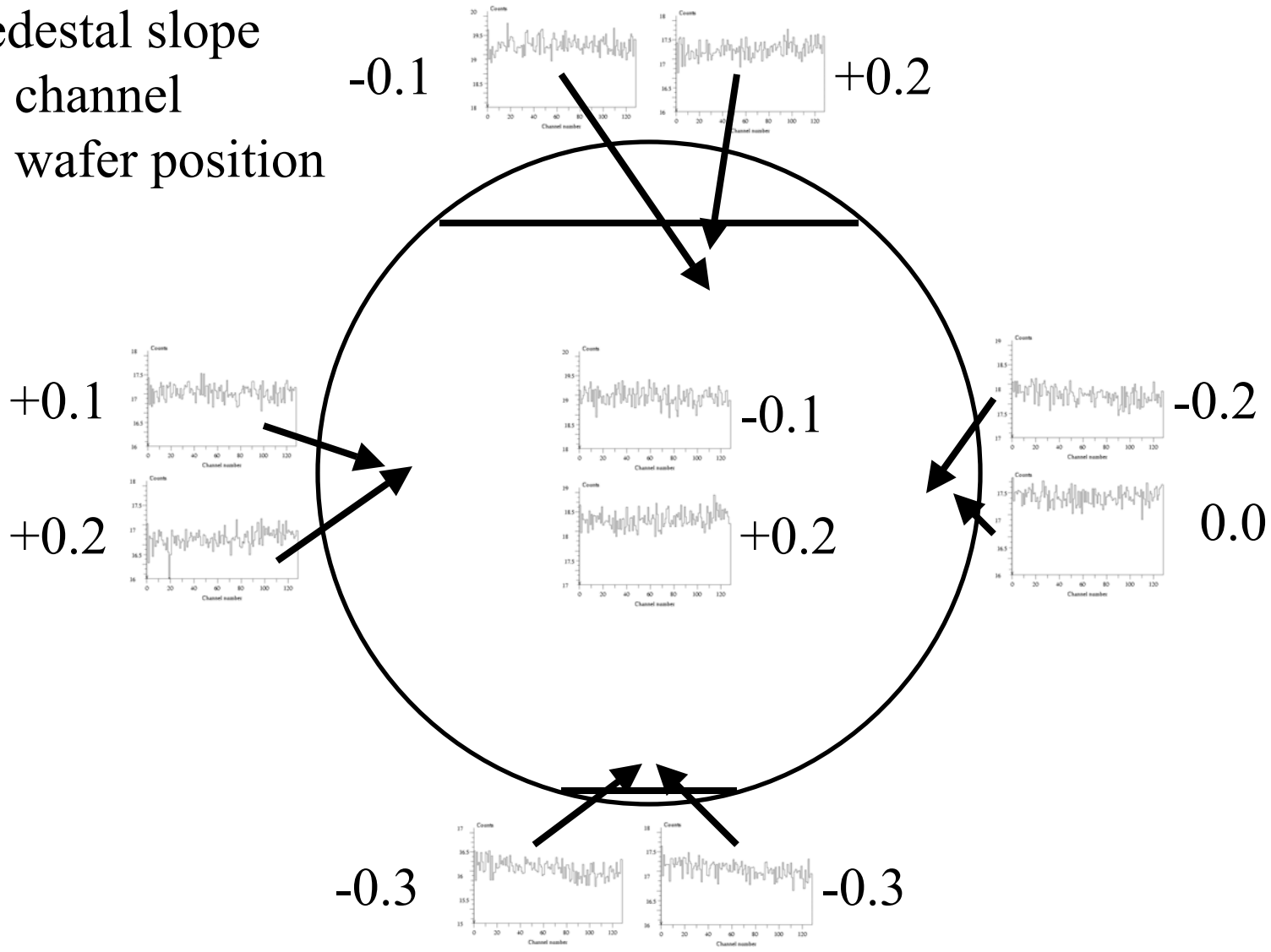


Pedestal vs pipeline cell for a single channel during various operations. SVX4_V2 (older version) compared with SVX4_2b (newer version). small slope over 46 pipeline cells is observed. Small coupling of chip operation into pedestal readout.

SVX4_V2

SVX4_2b

Pedestal slope
vs channel
vs wafer position



SVX4_2a and _2b wafer probing

- 11/11 initial devices looked good (basic functionality) – before grinding and plating
- 56 devices looked at after grind/plating
  - 2 bad (current draws)
  - 10 with one or two bad channels
  - 4 with higher pedestal (needs investigation)
- Note: many of the 56 devices were close to the wafer's edge

SVX4_2a SVX4_2b wafer probing results

- 7/8 of the 1st wafer tested (398 devices)
- A 2nd wafer probed (454 devices)
- Only 4 devices found non-functional
  - 2 bad current draws
  - 2 bad readout
- Next to examine:
  - Bad channels
  - Bad pipeline cells